

(19) Japan Patent Office (JP)

(12) Publication of Patent Application (A)

(11) Patent Application Publication No.:

H6-250224

5

---

(51)Int. Cl. <sup>5</sup> Indications	Identification Code	JPO File Number	FI	Technical
G02F 1/ 136	500	9018- 2K		
1/ 1335		7408- 2K		
10 1/ 1339	500	8507- 2K		
1/ 1345		8707- 2K		
		9056- 4M	H01L 29/ 78	311

A

Request for Examination: Not Requested Number of Claims: 5 FD

15

(6 pages in total) Continued on Last page

---

(21) Application Number: H5-59668

(22) Filing Date: H5 (1993) February 24

(71) Applicant: 000002185

20

Sony Corporation

6-7-35, Kitashinagawa, Shinagawa-ku, Tokyo

(72) Inventor: Takuo Sato

5-1 Noguchikita, Kokubu-shi, Kagoshima

c/o Sony Kokubu Corporation

25

(74) Agent: Harutoshi Suzuki, Attorney

---

(54) LIQUID CRYSTAL DISPLAY DEVICE

(57) [Abstract]

[Purpose] To maintain uniformity of a liquid crystal cell gap and to prevent light leakage by suppressing the hillocks of a guard ring metallic layer provided in an active matrix type liquid crystal display device.

[Structure] The active matrix liquid crystal display device has a first substrate 1, a second substrate 21 provided opposite to the first substrate, and a liquid crystal layer 16 held between the first and second substrates. A display region including a matrix type pixel electrode 11 and thin-film transistors each driving a pixel electrode 11 is formed on the first substrate 1. Further, a guard ring metallic layer 9 enclosing the display region is provided on the first substrate 1. Rugged level differences 17 are provided along a lower part of the guard ring metallic layer 9 to prevent the generation of hillocks. The rugged level differences 17 are formed at intervals of 0.5 mm or less. The rugged level differences 17 are provided in an interlayer insulating film 6 interposed between the first substrate 1 and the guard ring metallic layer 9.

[Claims for the Patent]

[Claim 1] A liquid crystal display device comprising:

a first substrate;  
a second substrate provided opposite to the first substrate; and  
liquid crystal held between the first substrate and the second substrate,  
wherein on the first substrate, a display region having matrix type pixel electrodes and thin film transistors each driving a pixel electrode is formed,  
a metallic layer enclosing the display region is provided on the first substrate, and  
rugged level differences are provided along a lower part of the metallic layer.

[Claim 2] A liquid crystal display device according to claim 1,  
wherein the rugged level differences are formed at intervals of 0.5 mm or less.

[Claim 3] A liquid crystal display device according to claim 1,

wherein the rugged level differences are provided in an interlayer insulating film interposed between the first substrate and the metallic layer.

[Claim 4] A liquid crystal display device according to claim 1,

5 wherein the metallic layer is provided to be aligned to a sealing material for joining the first and second substrates together.

[Claim 5] A liquid crystal display device according to claim 1,

wherein the metallic layer is formed from the same material as an extraction electrode for external connection.

10 [Detailed Description of the Invention]

[0001]

[Industrial Application Field]

The present invention relates to an active matrix liquid crystal display device, in which a plurality of pixels each having a switching transistor are arranged in a matrix. In particular, the invention relates to a guard ring structure enclosing a display region.

15

[0002]

[Prior Art]

In order to clarify the background, the structure of a conventional active matrix liquid crystal display device will be briefly described with reference to FIG. 3. As shown in the diagram, a thin film transistor (TFT) 101 for driving a pixel, a gate line 102 for supplying a selection signal to the TFT 101, a signal line 103 for supplying an image signal to the TFT 101, a pixel electrode 104 and the like are formed on a glass substrate 100. Further, a guard ring metallic layer 105 is formed to enclose the display region enclosing the TFT 101 and the pixel electrode 104. A counter substrate 106 is bonded to the glass substrate 100 using a sealing material 107 with a predetermined gap therebetween. A counter electrode 108 is formed on the inner surface of the counter substrate 106. A liquid

20

25

crystal layer 109 is held between the lower glass substrate 100 and the upper counter substrate 106, and is for example, formed from twisted nematic liquid crystal. The sealing material 107 is provided along the periphery of either the substrate 100 or 106 such that it is aligned to the guard ring metallic layer 105.

5 [0003]

The metallic layer 105 encloses the inside display region, and electrically protects the TFT 101 as a guard ring. In addition, wiring level differences or the like on the surface of the glass substrate 100 are absorbed for planarization by aligning the metallic layer to the sealing material 107; thus, the thickness of the liquid crystal layer 109 is made  
10 uniform. The guard ring metallic layer 105 has functions of not only protecting TFTs or the like from electrostatic damage in a manufacturing process but also controlling the liquid crystal cell gap uniformly; thus, yield and display image quality can be improved. In addition, the guard ring metallic layer 105 can also serve as a light blocking layer.

[0004]

15 However, in the case of the above conventional structure, the guard ring is constituted by a metallic layer 105 formed on a relatively flat surface of the glass substrate 100, and so-called hillocks are easily generated if heat treatment is applied in a post-process, which is a problem. The hillocks are due to electromigration or stress migration of a material forming the metallic layer 105, and protruding hillocks are generated at the metal  
20 grain boundary portion. When hillocks are generated, planarity of the surface of the metallic layer 105 is impaired, and the thickness of the sealing material 107 changes, which is a cause of a liquid crystal cell gap defect. Further, the hillocks may impair light blocking properties of the metallic layer 105, which may be a cause of so-called light leakage. The light leakage of the guard ring does not directly affect display image  
25 because it is away from the display region having a pixel electrode or the like; however, in the case of incorporating a backlight or the like, light leakage from around the display

region would deteriorate the display quality. The generation of the hillocks is a major problem particularly when aluminum is used as a constituent of the metallic layer 105. As to the metal aluminum, hillocks are easily generated even in the case of using heat treatment of a relatively low temperature of approximately 400 °C.

5 [0005]

[Means to solve the Problems] In view of the above described problems of the conventional art, it is an object of the present invention to provide a liquid crystal display device without liquid crystal cell gap defects and generation of light leakage, in which generation of hillocks can be suppressed even when a guard ring metallic layer is heat treated. In order  
10 to achieve the objects, the following measures were taken. Specifically, a liquid crystal display device in accordance with the present invention includes a first substrate, a second substrate provided opposite to the first substrate, and liquid crystal held between the first substrate and the second substrate, as basic components. On the first substrate, a display region having matrix type pixel electrodes and thin film transistors each driving a pixel  
15 electrode is formed. As a feature of the invention, a measure is taken in which a metallic layer enclosing the display region is provided on the first substrate, and rugged level differences are provided at a lower part of and along the metallic layer. Preferably, the rugged level differences are formed at intervals of 0.5 mm or less. The rugged level differences are for example, provided in an interlayer insulating film interposed between  
20 the first substrate and the metallic layer. Further, the metallic layer is provided to be aligned to a sealing material for bonding the first and second substrates together. In addition, the metallic layer is formed from the same material as an extraction electrode for external connection.

[0006]

25 [Operation] In accordance with the present invention, along a lower part of a guard ring metallic layer enclosing a display region, for example, rugged level differences are

provided at intervals of 0.5 mm or less. When the rugged level differences exist, the material forming the metallic layer hardly migrates; thus, generation of hillocks can be suppressed. Therefore, even when a sealing material is provided to be aligned to the guard ring metallic layer, planarity of the metallic layer surface can be maintained, which  
5 reduces liquid crystal cell defects. Further, light leakage caused by hillocks can be improved. In contrast, when a guard ring metallic layer is provided over a large area of a relatively flat glass substrate surface as in conventional, migration easily occurs, which causes multiple hillocks.

[0007]

10 [Embodiment] Hereinafter, a suitable embodiment of a liquid crystal display device of the present invention will be described in detail with reference to drawings. FIG. 1 is a schematic cross-sectional view illustrating a basic structure of an active matrix liquid crystal display device of the present invention. As shown in the diagram, thin film transistors (TFTs) are formed and integrated on an insulating substrate 1 formed of glass,  
15 quartz, or the like. In order to simplify the diagram, only two TFTs, TFTs 2 and 3 are shown. One of the TFTs, TFT 2 is used for switching a corresponding pixel and the other, TFT 3 forms a driver circuit for sequentially selecting and driving a matrix array of pixels. Each TFT is formed from a polycrystalline silicon film 4 patterned into a predetermined shape. The polycrystalline silicon film 4 is formed to a thickness of 50 nm by LP-CVD,  
20 for example. A gate electrode G is formed over the polycrystalline silicon film 4 with a gate insulating film 5 formed of SiO<sub>2</sub> therebetween. Note that the gate electrode G of the pixel TFT 2 is extended from the gate line (not shown). The gate electrode G and the gate line are simultaneously formed from a 350 nm thick polycrystalline silicon film deposited by LP-CVD, which is doped with impurities. They are coated with a first interlayer  
25 insulating film 6. The first interlayer insulating film 6 is, for example, formed from a 600 nm thick PSG film deposited by AP-CVD. Further, an aluminum film is formed to a

thickness of 600 nm by sputtering, for example. The aluminum film is patterned into a predetermined shape to form a signal line 7, a wiring electrode 8, a guard ring metallic layer 9, and the like. The signal line 7 is electrically connected to a source region S of the pixel TFT 2 through a contact hole provided in the first interlayer insulating film 6.

5 Further, the wiring electrode 8 is electrically connected to a source region S and a drain region D of the pixel TFT 3 similarly through a contact hole provided in the first interlayer insulating film 6. A second interlayer insulating film 10 is formed over the aluminum film. The second interlayer insulating film 10 is, for example, formed from a PSG film deposited by AP-CVD to a thickness of 400 nm. Furthermore, a transparent conductive film of ITO  
10 or the like is formed thereon to a thickness of 150 nm by sputtering. The transparent conductive film is patterned into a predetermined shape to form a pixel electrode 11. The pixel electrode 11 is electrically connected to a drain region D of the pixel TFT 2 through a contact hole provided in the second interlayer insulating film 10 and the first interlayer insulating film 6.

15 [0008] A counter substrate 21 is provided opposite to the insulating substrate 1 with a predetermined gap therebetween. The counter substrate 21 is bonded to the insulating substrate 1 with a sealing material 12. The sealing material 12 is provided to be aligned to the guard ring metallic layer 9 by screen printing or the like. On an inner surface of a counter substrate 21, a black mask 13 patterned into a predetermined shape, and a counter  
20 electrode 15 with an insulating film 14 therebetween are formed. The black mask 13 is formed by patterning so as to shade the TFT 2 and TFT 3. A region other than the pixel electrode 11 is covered with the black mask 13 formed on the counter substrate 21 side and the guard ring metallic layer 9 formed on the insulating substrate 1; thus, a desired light blocking structure can be obtained. Lastly, the liquid crystal layer 16 is enclosed and  
25 maintained between the counter substrate 21 and the insulating substrate 1. The liquid crystal layer 16 is formed for example, from twisted nematic liquid crystal.

[0009] The guard ring metallic layer 9, which is a feature of the present invention is provided so as to enclose the display region having the TFT 2 and the pixel electrode 11. As described above, the guard ring metallic layer 9 is formed from a material of 600 nm thick aluminum the same material as the signal line 7 and the wiring electrode 8 and they are patterned simultaneously. The guard ring metallic layer 9 electrically protects the TFT 2 and the TFT 3 inside and is aligned to the sealing material 12 so that it also serves to planarize the bonding region. Along a lower part of the guard ring metallic layer 9, the rugged level differences 17 are provided. In this example, the rugged level differences 17 are provided in the first interlayer insulating film 6 interposed between the insulating substrate 1 and the metallic layer 9. With the provision of the rugged level differences 17 in between, migration of aluminum is suppressed to prevent generation of hillocks.

[0010] FIG. 2 is a plan view of an active matrix liquid crystal display device shown in FIG. 1. As shown in the diagram, pixel electrodes 11 are arranged in a matrix inside the display region 18 enclosed by the guard ring metallic layer 9 to form each liquid crystal pixel. Pixel TFTs 2 are each connected to the pixel electrodes 11. Gate lines 19 are each connected to the gate electrode of each pixel TFT 2, and similarly, signal lines 7 are each connected to the source electrode thereof. The plurality of gate lines 19 are connected to a vertical driver circuit 22; meanwhile, the plurality of signal lines 7 are connected to a horizontal driver circuit 23. The vertical driver circuit 22 selects pixel TFTs 2 through the gate lines 19 line sequentially, and the horizontal driver circuit 23 supplies image signals to a corresponding pixel electrode 11 using the signal lines 7 through a selected pixel TFT 2. The vertical driver circuit 22 and the horizontal driver circuit 23 each include a TFT 3 as a structural element.

[0011] Extraction electrodes 24 for external connection are formed at the periphery of the insulating substrate 1 and are connected to the vertical driver circuit 22 and the horizontal driver circuit 23 so as to intersect with the guard ring metallic layer 9. The extraction



electrodes 24 are formed from the same aluminum film as the guard ring metallic layer 9. In order to make understanding easier, an enlarged pattern shape of the intersection of the extraction electrodes 24 and the guard ring metallic layer 9 are shown. As shown in the diagram, a band of the guard ring metallic layer 9 is partially eliminated, and the extraction electrodes 24 extend over the area. The separated metallic layers 9 are connected to each other for example with a polycrystalline silicon film 25 patterned into a predetermined shape. The polycrystalline silicon film 25 is formed simultaneously with the gate electrode and the gate line and is insulated from the metallic layers 9 and the extraction electrodes 24 by the first interlayer insulating film. The extraction electrodes 24 are laid from the vertical driver circuit 22 and the horizontal driver circuit 23 to the outside of the sealing material for making an electrical connection to the external. Therefore, the middle parts of the extraction electrodes 24 cross over the seal region. In this structure, the guard ring metallic layers 9 are provided in the vicinity of both sides of each extraction electrode 24 in the seal region. Consequently, the whole seal region can be approximately planarized. Thus, the extraction electrode 24 and the guard ring metallic layer 9 are formed of aluminum having the same thickness, and level difference is eliminated.

[0012] Along the band of the guard ring metallic layer 9, rugged level differences 17 are provided. In this example, the rugged level differences 17 are formed from openings of 100  $\mu\text{m}$  square provided in the first interlayer insulating film disposed at the lower part of the metallic layer 9. The openings are arranged at intervals of 100  $\mu\text{m}$ . Such openings can be formed by selective etching of the first interlayer insulating film. The rugged level differences 17 relax stress inside the aluminum film; thus, migration hardly occurs. For example, even if a heat treatment at approximately 400  $^{\circ}\text{C}$  is added after the step of depositing the aluminum film, no aluminum hillocks are generated in the guard ring region. In this manner, according to the present invention, even when a guard ring formed of metal is adopted and heat treatment is added, generation of hillocks can be suppressed; thus, a

liquid crystal display device without liquid crystal cell gap defects and light leakage can be provided.

[0013] On the other hand, a liquid crystal display device is formed in the same manner as the above embodiment other than the fact that openings are not formed in the first insulating film disposed at a lower part of the guard ring metallic layer formed of aluminum, as a comparative example. In this case, many hillocks were generated in the guard ring metallic layer in heat treatment of the later step. Therefore, good products were hardly obtained due to liquid crystal cell gap defects and light leakage; accordingly, yield was significantly low.

[0014] Note that in the above embodiment, an aluminum film having a thickness of 600 nm was used as the guard ring metallic layer; however, the present invention is not limited thereto. A material having sufficiently low resistance, which is the same as the external extraction electrodes may be used. The light blocking properties of the guard ring metallic layer may correspond to a transmittance of 1 % or less, preferably, 0.1 % or less in a visible light region (from 400 nm to 700 nm). As the material, other than aluminum (Al), a metal such as Cr, Ni, Ta, Ti, W, Cu, Mo, Pt, or Pd; an alloy thereof; a silicide thereof; or the like can be used. The thickness depends on each material to satisfy a predetermined light blocking property and is generally 50 nm or more.

[0015] Further, in this embodiment, as shown in FIG. 2, the configuration of the rugged level differences was such that square openings of 100  $\mu\text{m}$  square each are arranged at intervals of 100  $\mu\text{m}$  at the lower part of the guard ring metallic layer; however, the present invention is not limited thereto. Generally, the rugged level differences may have any shape as long as they can be arranged at intervals of 0.5 mm or less. Supposing if they are arranged at intervals of 0.5 mm or more, effect of migration suppression is reduced. As another example, stripe shaped grooves having openings of 500  $\mu\text{m}$  square at intervals of 50  $\mu\text{m}$  may be formed. Alternatively, circular openings having a diameter of 100  $\mu\text{m}$  may

be formed.

[0016] Note that in this embodiment, polycrystalline silicon is used for the semiconductor layer, the gate electrode, and the gate line of a TFT, SiO<sub>2</sub> is used for the gate insulating film, and aluminum is used for the signal line; however, the present invention is not limited thereto. For example, amorphous silicon may be used for the semiconductor layer of the TFT. For example, silicide, polycide, or a metal such as Ta, Al, or Cr may be used for the gate electrode and the gate line. For example, SiN, tantalum oxide, or the like can be used for the gate insulating film. For example, Ta, Cr, Mo, Ni, or the like can be used for the signal line. In addition, the present invention can be naturally applied to an active matrix liquid crystal display device using any one of planar, staggered, and inverted staggered thin film transistors.

[0017]

As described above, according to the present invention, rugged level differences are provided at a lower part of a guard ring metallic layer enclosing a display region at intervals of at least 0.5 mm or less. The rugged level differences relax stress; thus, migration hardly occurs and generation of hillocks is suppressed. Therefore, planarity of the guard ring metallic layer at the interface with a sealing material can be maintained and occurrence of liquid crystal cell gap defects can be prevented. Further, light leakage of the guard ring metallic layer due to hillocks, which is a conventional problem, can be greatly improved. Even if heat treatment is added after forming the guard ring metallic layer, hillocks are not generated and a liquid crystal display device without liquid crystal cell gap defects and light leakage can be provided.

[Brief Description of the Drawings]

[FIG. 1] A cross-sectional view illustrating a structure of an active matrix liquid crystal display device of the present invention.

[FIG. 2] A plan view of the active matrix liquid crystal display device shown in FIG. 1.

[FIG. 3] A cross-sectional view illustrating a structure of a conventional active matrix liquid crystal display device.

[Reference Numerals]

1: insulating substrate, 2: TFT, 3: TFT, 4: polycrystalline silicon film, 5: gate insulating film,  
5 6: first interlayer insulating film, 7: signal line, 8: wiring electrode, 9: guard ring metallic  
layer, 10: second interlayer insulating film, 11: pixel electrode, 12: sealing material, 13:  
black mask, 15: counter electrode, 16: liquid crystal, 17: rugged level differences, 18:  
display region, 19: gate line, 21: counter substrate, 22: vertical driver circuit, 23: horizontal  
driver circuit, 24: extraction electrode, 25: polycrystalline silicon film.

10

---

Continued from Front Page

(51)Int. Cl. <sup>5</sup>	Identification Code	JPO file number	FI	Technical
Indications				
H01L 29/784				